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(54) Mixed typology output stage.

(57) An output power stage composed of a pair of transistors driven in phase opposition and wherein the pull-up transistor is a PNP bipolar transistor and the push-down transistor is an n-channel FET has an outstandingly improved power handling capability per semiconductor area occupied, coupled with a large output voltage swing, without requiring the use of externally connected discrete boot-strap components. The "hybrid" output stage is fully complementary and the current-driven, bipolar, pull-up transistor may be driven through an auxiliary stage composed of a field effect transistor for substantially eliminating output power requisites of a signal amplification stage.

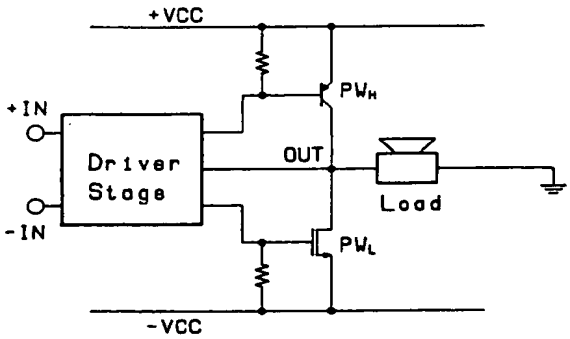

FIG.1

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The present invention relates to an output stage for an integrated power amplifier particularly suited for audio amplifiers.

The output stages of power amplifiers are normally designed for maximizing the dynamic excursion of the output voltage (output voltage swing), by reducing as much as possible voltage drops due to the series resistance of the active components (transistors) that form the output stage. There is an ample specific bibliography out of which the volume "Power Integrated Circuit", published by Mc.Graw Hill, in 1986, pages 9.28 - 9.35 may he cited.

A widely used technique in power output stages is that of realizing a "bootstrap" line, using for this purpose a relatively large capacitance, that may be externally connected to the IC pins, in order to obtain the maximum peak-to-peak variation of the output voltage. Unfortunately, this technique conflicts with a general IC design trend of eliminating or reducing the need of passive external components to a minimum.

The known configurations of a power output stage are amply reported in literature and substantially are those employing a pair of transistors operating in phase opposition, namely an NPN/NPN, PNP/NPN, pMOS/nMOS and nMOS/nMOS pair. Of course, the selection of one of the above configurations depends on the fabrication technology that is employed, which determines also the maximum reverse voltage that can be withstood by the devices (for example the maximum V_{CE} of bipolar junction transistors or the maximum V_{DS} of MOS transistors).

Bipolar NPN transistors notably suffer from the problem connected to the so-called "second breakdown" phenomenon. Also bipolar PNP transistors are affected by this phenomenon but in a lesser measure than NPN transistors.

On the contrary, DMOS transistors are notably exempt of this problem.

In a mixed technology fabrication process (BJT, CMOS and DMOS) or BCD process, the power MOS transistors that can be realized in a compatible manner with the other type of integrated structures, have internal resistance characteristics that typically show the following values:

(n-channel) DMOS : Ron = 0.5Ω x mm²
(p-channel) DMOS : Ron = 2.2Ω x mm²

In particular, the solution of using a complementaty pair of DMOS output transistors would appear an ideal choice, by considering also the advantage represented by the fact that the two output transistors would not need a driving current, being intrinsically voltage-controlled devices. However, a p-channel DMOS transistor requires an integration area that may be four times the integration area of an n-channel, complementary DMOS transistor, for the same Ron. Therefore the solution that employs a complementary pair of DMOS transistors is adopted only in a limited number of applications, where the relatively large silicon area requirement is not a problem.

On the other hand, the use of a (more compact) pair of transistors of the same polarity (that is noncomplementary), for example a pair of n-channel DMOS transistors, beside losing a portion equivalent to a VGS voltage of the maximum voltage swing of the output signal or otherwise requiring a bootstrap line, requires also a somewhat more complex driving circuit than the circuit that would be necessary for driving, in phase opposition, a complementary pair of output transistors.

There is a long felt need or utility of a complementary output stage with good breakdown characteristics that would not need externally connected bootstrap components and require a relatively large area of integration.

It has been found that in a normal BCD fabrication process it is possible to realize a bipolar PNP power transistor, having an internal resistance Ron of about 0.3Ω x mm², which can be satisfactorily used as the high side part of a complementary output power stage that employs as its low side part, an n-channel field effect transistor.

A so configured output stage is perfectly complementary and therefore does not reduces the output dynamics by a VGS (or by a VBE) and may be driven by a relatively simple stage.

The output stage has an intrinsically high voltage swing characteristic and does not need externally connected boostrap components. The use of power transistors of different technology (a bipolar transistor of the high side or pull-up part and a field effect transistor for the low side or push-down part), permits to reach an outstandingly good compromise between the extent of silicon area necessary for integrating the two power transistors, by exploiting the relatively small size of an n-channel DMOS structure and of a vertical, isolated collector, PNP structure and the driving power requisite, which is required only by the active pull-up element constituted by the bipolar PNP transistor.

According to an alternative embodiment of the output stage of the invention, the pull-up power element, constituted by a bipolar PNP transistor, is driven by a stage composed of a field effect transistor, for example a p-channel MOS transistor, of sufficient size to provide the driving power required by the bipolar output transistor.

According to an embodiment of the invention, the PNP transistor may be constituted by a complex structure that comprises the PNP and NPN transistors, the electrical behaviour of which can be

equated to that of an equivalent PNP transistor. This solution permits to further reduce the integration area, being the power NPN structure of the PNP equivalent complex structure capable of operating at a higher current density than a PNP structure and therefore requiring a reduced area of integration. Of course, in this latter case, the output voltage swing would be reduced by a VBE but this could be advantageously traded-off with a maximized saving of silicon area.

The different aspects and advantages of the output stage of the invention will become more evident through the following description of several embodiments and by referring to the annexed drawing, wherein:

Figure 1 is a circuit diagram of an output stage of the invention;

Figure 2 is a circuit diagram of an output stage of the invention, according to an alternative embodiment thereof;

Figure 3 is a more detailed circuit diagram of the output stage of Fig. 2.

With reference to Fig. 1, the output stage of the invention is essentially constituted by a pull-up power element PW_H, composed of a bipolar PNP transistor, and by a push-down power element PW_L, composed of a DMOS transistor. The collector of PW_H and the drain of PW_L are connected in common to an output node OUT of the amplifier. The complementary pair of transistors of the output stage is customarily driven by a suitable driving stage.

Of course, while the driving of the MOS transistor PW_L occurs essentially in a voltage mode, with a practically null driving power, the driving of the high side element of the push-pull output stage, that is of the bipolar PNP transistor PW_H, requires a certain driving current (base current).

An alternative embodiment of the output stage of the invention is shown in Fig. 2, wherein a MOS transistor M1 is employed for driving the bipolar PNP transistor PW_H, so as to prevent to load the relative output node of the driver stage.

A circuit diagram of the driver stage is depicted in Fig. 3. As may be observed, the driver stage may be realized with field effect transistors in a substantially symmetrical form. The high side part of the push-pull output stage, that is the power transistor PW_H (driven through the MOS M1) is driven by the amplifier composed of R3, M2, M3 and the current generator I1. The low side part of the push-pull output stage, composed of the n-channel DMOS transistor PW_L is driven by the amplifier composed of R4, M4, M5 and the current generator I2. In order to ensure compatibility to ground potential, the two resistances R1 and R2, connected between the IN- node and ground and between the IN-node and the load, respectively, determine the voltage gain.

Claims

1. An integrated output stage comprising a pair of transistors functionally connected between a positive and a negative supply rail, driven in phase opposition by a driver stage, characterized by the fact that a pull-up transistor of said pair is a PNP bipolar transistor and a push-down transistor of said pair is an n-channel field effect transistor.

2. An integrated output stage as defined in claim, characterized by the fact that said PNP transistor is driven by a stage comprising a p-channel field effect MOS transistor.

3. An integrated output stage as defined in claim 1, wherein said PNP transistor is an integrated, isolated collector, vertical transistor.

4. An integrated output stage as defined in claim 1, wherein said field effect transistor is a DMOS transistor.

5. An integrated output stage as defined in claim 1, wherein said PNP transistor is composed of a composite structure comprising a PNP transistor and an NPN transistor, electrically equivalent to a PNP transistor.

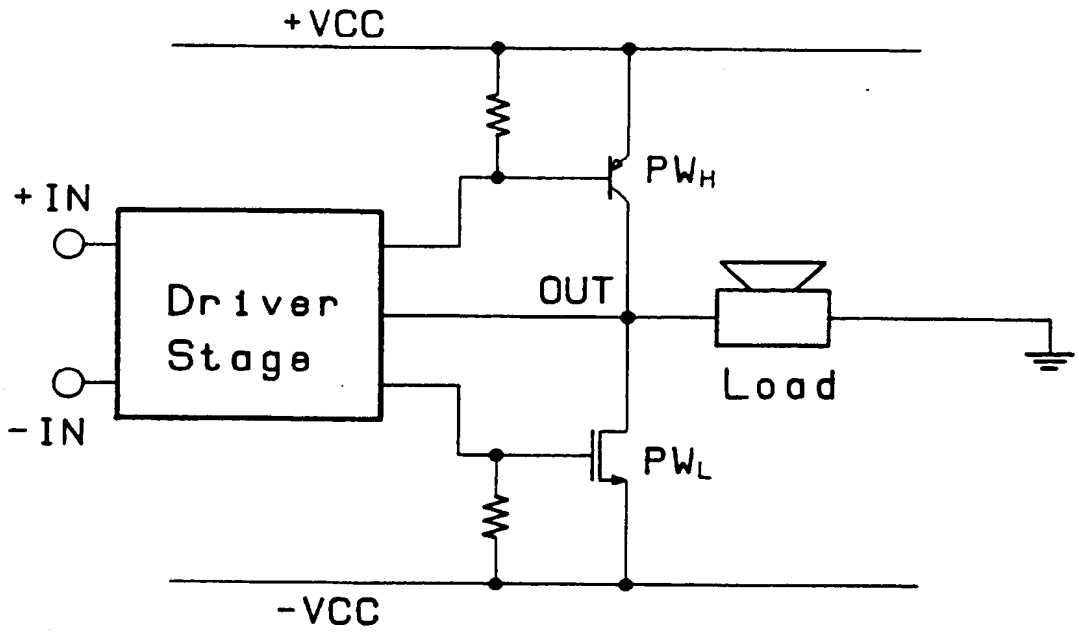
+VCC
+IN
-IN
Driver Stage
PWH
OUT
Load
PWL
-VCC

FIG.1

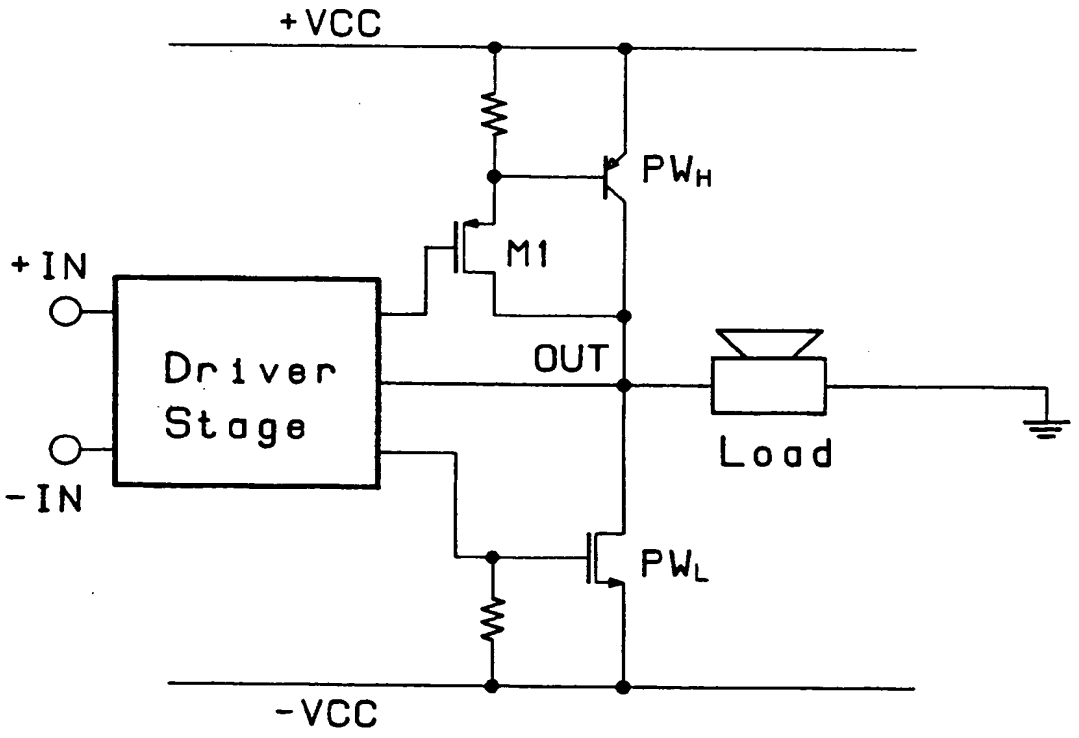
+VCC
+IN
-IN
Driver Stage
PWH
M1
OUT
Load
PWL
-VCC

FIG.2

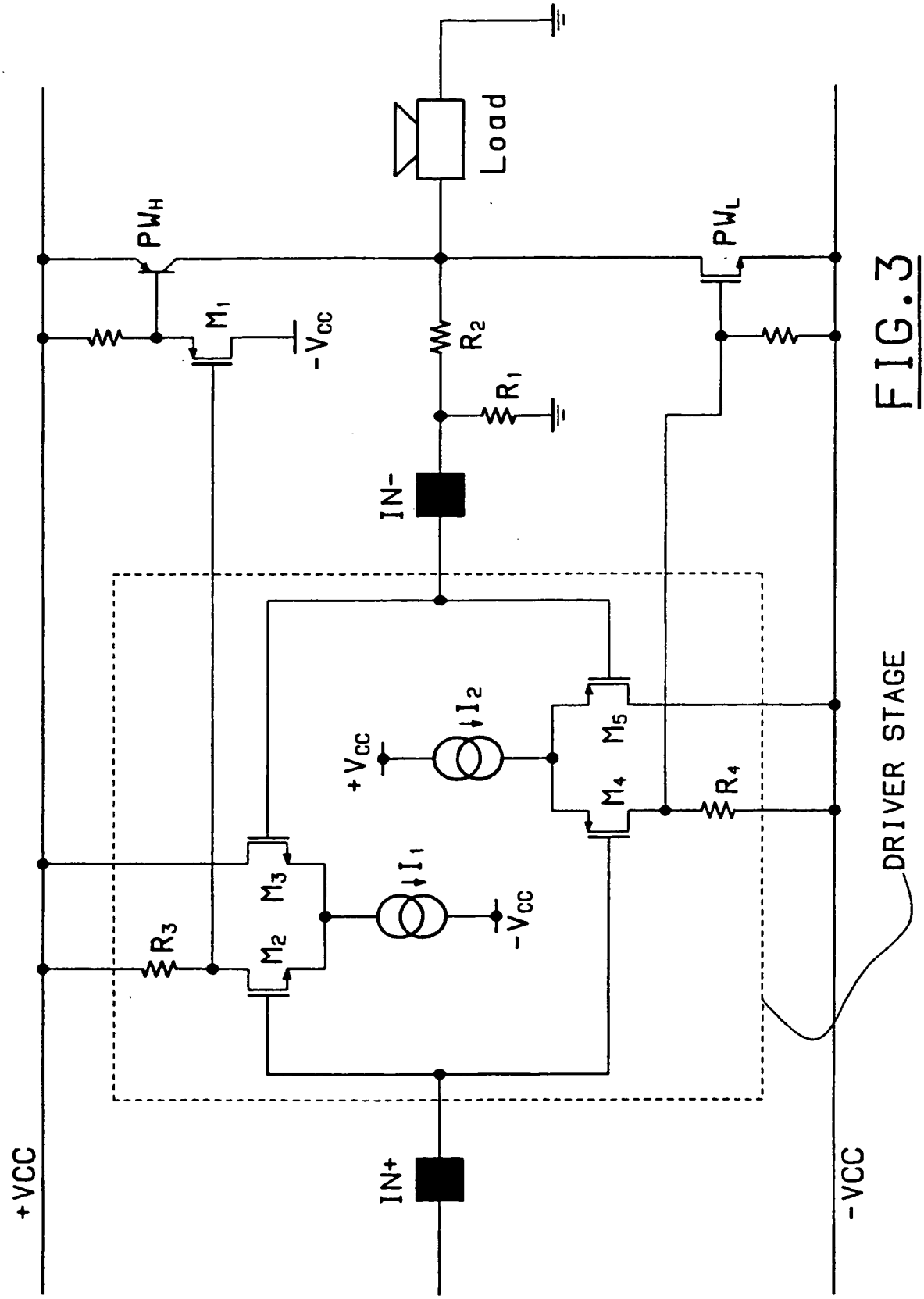

FIG.3

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EUROPEAN SEARCH REPORT

Application Number
EP 93 83 0492

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP-A-0 349 954 (MOTOROLA) * column 2, line 40 - column 4, line 27; figure 1 *	1	H03F3/30
A	US-A-5 028 881 (J.H. SPENCE) * column 2, line 67 - column 5, line 45; figure 1 *	1,2	
A	US-A-4 588 960 (C.A. SALAMA ET AL) * column 2, line 61 - column 4, line 15; figures 3,4 *	1,5	
A	1990 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, vol.4, 1 May 1990, SHERATON L.A. pages 3201 - 3204, XP163513 J. AHO ET AL 'NOISE OPTIMIZATION OF BICMOS OPERATIONAL AMPLIFIERS' * page 3202, right column; figure 1 *	1,2	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6) H03F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 April 1994	Tyberghien, G

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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